

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.

826.1767

APPLICATION NO.

10542 U.S. PTO

09/985768

## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

FIRST NAMED INVENTOR

Kwame Osei BOATENG

FILING DATE

November 5, 2001

GROUP ART UNIT

2825

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
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## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO	
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

## OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

95	AM	K. O. Boateng, H. Takahashi and Y. Takamatsu, "Diagnosing Delay Faults in Combinational Circuits Under the Ambiguous Delay Model," IEICE Transaction on Information and Systems, Vol. E82-D, No. 12, pp. 1563-1571.
15	AN	K. O. Boateng, H. Takahashi, and Y. Takamatsu, "Multiple Gate Delay Fault Diagnosis Using Test-Pairs for Marginal Delays," IEICE Transaction on Information and Systems, Vol. E81-D, No. 7, pp. 706-715.
15	AO	N. Yanagida, H. Takahashi and Y. Takamatsu, "Multiple Fault Diagnosis By Sensitizing Input Pairs," IEEE Design and Test of Computers, Vol. 12, No. 3, pp. 44-52.

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DATE CONSIDERED

6/14/05

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	<b>FIRST NAMED INVENTOR</b> Kwame Osei BOATENG	
	<b>FILING DATE</b> November 5, 2001	<b>GROUP ART UNIT</b> 2820

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	AJ							
	AK							
	AL							

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VS	AM	I. Pomeranz and S. M. Reddy, "On Test Compaction Objectives for Combinational and Sequential Circuits," Proceedings of IEEE International Conference on VLSI Design, pp. 279-284.
VS	AN	S. Kajihara and K. Saluja, "On Test Pattern Compaction Using Random Pattern Fault Simulation," Proceedings of IEEE International Conference on VLSI Design, pp. 464-469.
VS	AO	I. Hamzaoglu and J. H. Patel, "Test Set Compaction Algorithms for Combinational Circuits," Proceedings of ACM International Conference on CAD, pp. 283-289.

<b>EXAMINER</b> WTHE SIER	<b>DATE CONSIDERED</b> 6/14/05
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17	AM	M. S. Hsiao and S. T. Chakradhar, "Partitioning and Reordering Techniques for Static Test Sequence Compaction of Sequential Circuits," Proceedings of the 7 <sup>th</sup> IEEE Asian Test Symposium, pp. 452-457.
VS	AN	M. S. Hsiao and S. T. Chakradhar, "State Relaxation Based Subsequence Removal for Fast Static Compaction in Sequential Circuits," Proceedings of Design, Automation, and Test in Europe Conf., pp. 557-582.
VS	AO	M. S. Hsiao and E. M. Rudnick and J. H. Patel, "Fast Algorithms For Static Compaction of Sequential Circuit Test Vectors," Proceedings of IEEE VLSI Test Symposium, pp. 188-195.

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